ANALOG MODULES, INC.

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Specialists in Analog and Laser Electronics

MODEL 611A FAST PEAK PULSE STRETCHER
APPLICATION AND OPERATING NOTES

1.0 GENERAL

The 611A Fast Peak Pulse Stretcher module is designed to grab the instantaneous peak value of a narrow pulse or transient event and preserve it for later analysis. This is accomplished with two peak and hold stages operated in series. Each peak and hold has its own reset to increase system flexibility. A fast input gate is included to permit user selection of the pulse to be captured.

The 611A provides for a high impedance using a FET buffer. It is also available optimized for wider pulses (>50nS).

2.0 CIRCUIT DESCRIPTION

2.1 General

The input pulse is compared with the value stored in capacitor C by a very high speed one-way amplifier. If the stored value is less than the input, then a charging current flows to force the voltage on the capacitor to be equal to the input. When the input voltage falls, the one-way amplifier is disconnected and charge remains on the capacitor until slowly dissipated by leakage currents. By this process, the capacitor retains the peak value of the input. Repeating this function in a second stage stretches the peak value of the pulse to many seconds. In the second stage, a larger capacitor is used to provide longer hold times. Each capacitor is buffered by a high-impedance FET amplifier to ensure low leakage.

2.2 Reset

A reset is provided for each stage. A positive pulse on the reset terminal turns on the high speed NPN transistor to discharge the storage capacitor. Reset 1 (RST 1) has an input impedance of 1K in series with a 1000pf capacitor to provide DC level shifting to -5V, as well as to prevent a situation where the reset transistor is permanently turned on resulting in a large continuous current flow.

The first stage storage capacitor has a natural decay rate of approximately 0.55V/mS.This stage automatically resets in under 10mS. When a reset pulse of >2.5V is applied to RST 1, the reset time rate is 0.25V/nS, allowing for a complete first stage reset in approximately 16nS. The second stage capacitor has a decay rate of less than 0.1V/Sec., typically 0.015V/Sec. The set-up time for this capacitor to charge to the value stored in stage 1 is approximately 1μs. The reset time rate is 0.7V/μs, i.e., a total reset time from 4 volts of 5.7μs. A 15μs reset time is recommended and this time will be affected by the magnitude of the rest voltage on RST 2. For the fastest reset times, apply a +5 volt pulse. The input impedance of RST 2 is >2.2K in series with a 0.1μF capacitor.

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3.0 APPLICATIONS OF RESET

3.1 For storing a continuous peak value which may be read asynchronously, no reset connection is necessary. The first stage will set up to waveform peaks and decay in <10mS. The second stage will set up to these peaks about 1μs later and will hold their value, decaying naturally at about 15mV/second typical.

3.2 To measure events occurring at a rate of less than 100Hz (10mS), RST 1 may be left disconnected and allowed to reset automatically. RST 2 would normally be reset by a 15μs pulse just prior to the expected event or just after sampling of the output. For example, for a 25pps laser, RST 2 may be fed from the laser trigger pulse adjusted to 15μs. The laser output may occur 100μs later and set up the new stored value. The output voltage will represent a box-car waveform at zero for only 75μs and holding the value of the latest pulse for 39.925mS. This could drive a display meter directly or with suitable scaling.

3.3 To measure events at more than 100Hz, the RST 1 and RST 2 may be linked together. The reset source must be capable of driving 680 ohms. Here both resets are simultaneously operated to avoid an incomplete decay of the first stage capacitor being sensed by the second stage after a natural decay type of reset.

3.4 To process multiple pulses closely separated in time, RST 1 may be operated by a real-time decision-making circuit. For example, to sense the last pulse in a train, a fast comparator may detect each pulse and provide a RST 1 to destroy the previous data, retaining the last pulse only, for the second stage to sense. If the pulse train width exceeds the set up time of the second stage, then a RST 2 pulse should be generated after the last pulse to ensure that the second stage has not stored a higher previous value. A delay time of tens of nanoseconds may be needed to ensure that the RST 1 has gone before the pulse of interest arrives. Knowing the set-up and reset characteristics of each stage, variations of this theme may be arranged to suit the circumstances.

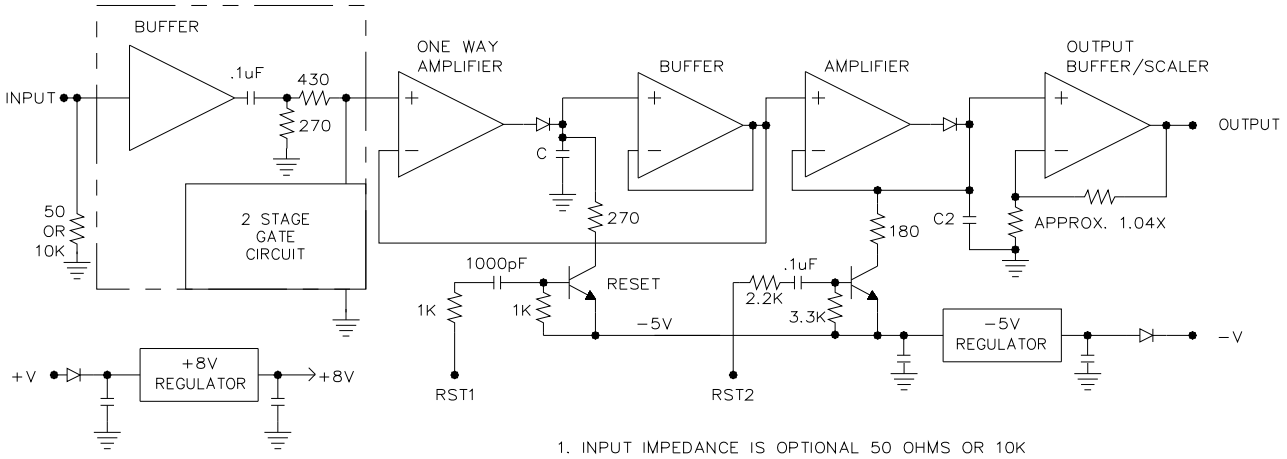
4.0 OPERATING NOTES

The 611A-2 has an additional ac-coupled FET buffer and shunt gate in series with the input. The input impedance is set by the value of resistor R1 connected from the input to ground and is normally 50 ohms or 10K. The output of the FET buffer is AC coupled via 0.1μF and 270 ohm resistor to ground. Pulses of more than 1μs may be partially differentiated and high duty cycle waveforms may reduce their DC amplitude values due to the effect of AC coupling. In these cases, consult the factory before ordering a 611A. The AC coupling is used to remove the FET offset voltage. The output of the FET buffer is fed to a 2 stage shunt gate which can attenuate the input signal by approximately 60dB voltage. The GATE input impedance is 910Ω.. A high (+2.5 to +5V) on the GATE turns the shunt switch ON to attenuate the signal. The switch turn on/turn off times are 5/15nS approximately depending on the drive level. This gate is useful for preventing spurious signals from being stored. The gate is DC coupled and may be held ON (closed).

Do not exceed 5V swing on the input between pulse peak and most negative baseline value since deterioration of the input transistors is possible with excessive voltage differential.

The 611A has reverse polarity protection on the power lines using series diodes.

The output is a low-impedance source from an operational amplifier connected as a buffer. Current is limited to 10mA or so. Consult the factory for applications requiring more current.



1. INPUT IMPEDANCE IS OPTIONAL 50 OHMS OR 10K

P3636_2.DWG

611A EQUIVALENT SIMPLIFIED CIRCUIT